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RESEARCH ARTICLE

A NOVEL CONTROL STRATEGY OF INDIRECT MATRIX CONVERTER IMPLEMENTED IN DFIG CONTROLLED WECS

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ABSTRACT

This paper discusses a control scheme of Indirect Matrix Converter which includes space vector modulation to stabilize the frequency variations. The terminal voltage and frequency of any synchronous machine can be controlled easily with this scheme. The proposed method leads to reduction of harmonics and losses predominantly increasing the efficiency of output. More over the control strategy is also very much flexible in their operation at any rated power. This work is mainly focused on the Matlab/Simulink implementation of SVM technique with Zero current switching for IMC. The novelty of this work is that a detailed analysis of directly AC to AC conversion with no energy storage element has been done and the SVM technique for IMC is implemented in Matlab/Simulink embedded system. The techniqe has been successfully implemented in wind energy conversion system and results have been analyzed.

INTRODUCTION

The Cyclo-converters are direct AC to AC converter without any DC-Link passive component in between. The demerits of cyclo-converter are requirement of large number of switching devices and complex control strategies for large 3 phase Cyclo-converter. Further, using Cyclo-converters the output frequency can be varied only to 1/3rd of the input frequency. In Matrix Converter topological scheme, there is no requirement of DC-Link storage elements. Further, it has a unique inherent bi-directional power flow capability. By using proper modulation strategies, desirable Sinusoidal output voltage can be generated by using this converter. Further, the input power factor can be fully controlled. The Matrix Converter technology can be used in all the Variable speed Drives. Now a days wind turbines are subjected to variation of load and impact of frequent change in wind speed with respect to the nonlinear behaviour of nature. Induction motors are frequently used in real world for industrial drive applications. Due to the advantage of bidirectional power flow and controllable power factor the IMC can replace the conventional back to back converter which has been experimentally verified.

TOPOLOGICAL SCHEME OF IMC

The control strategy of IMC requires coordination between the control of rectifier and inverter Stage unlike VBBC.

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The Space Vector based control strategy for MC gives better performance compared to carrier based control strategies. Further, the zero current switching of IMC can be easily achieved in Space Vector based control strategy. The advantage of zero current switching compared to forced commutation process is that the switching loss is less. A major breakthrough in the field of reduced and less complex switching strategy of IMCs was brought by Kolar and Ertl with the development of SMC in 2001. To understand this reduction in the switches, a detailed study has been done considering a single phase leg of the IMC as shown in figure. This leg of IMC is considered to be connected to the Input phase "a". This phase "a" is connected to the DC link through the switch Spa and Sap to the positive DC link and Sna and San to the negative DC link. The switches in this topology are arranged in such a manner that bi-directional power flow can take place for both positive and negative DC-Link Voltages. The fig. 2.1(1) and fig. 2.1(2) shows the condition when the DC-Link Voltage is positive and the current direction is positive. In fig. 2.1(1) the current flows from the Rectifier side to the Inverter side through Sap and Dap. In fig. 2.1(2) the current from Inverter side enters Rectifier side phase "a" through Dna and Sna. The fig. 2.1(3) and fig. 3.3(4) shows the condition when the DC-Link Voltage is negative and the current direction is negative. In fig. 2.1(4) the current flows from the Rectifier side to the inverter side through Dan and San. In fig. 2.1(3) the current from Inverter side enters Rectifier side phase "a" through Spa and Dpa. So, fig. 2.1 explains the bi-directional four quadrant power flow

capability of IMC. At this point there is another important concept to note that the inverter stage of the IMC can handle only positive DC-Link polarity, but the four quadrant switch current source type rectifier is capable of generating both positive and negative DC Link voltage polarities. For the inverter to work with negative DC-Link polarity the arrangement of the switches has been reversed which is not practically feasible.

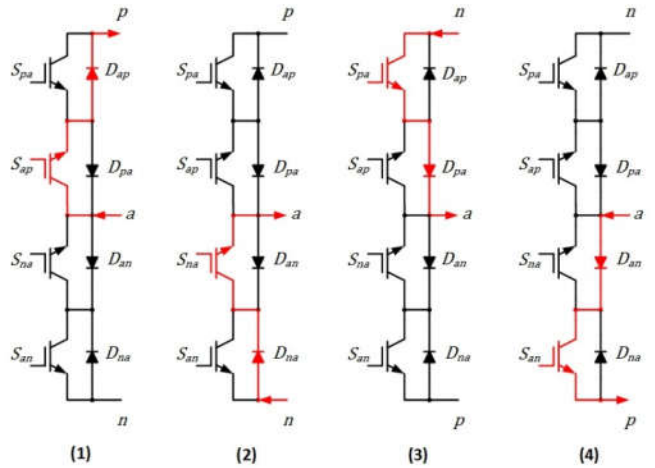

Fig. 2.1. Current flow for positive power flow in one leg

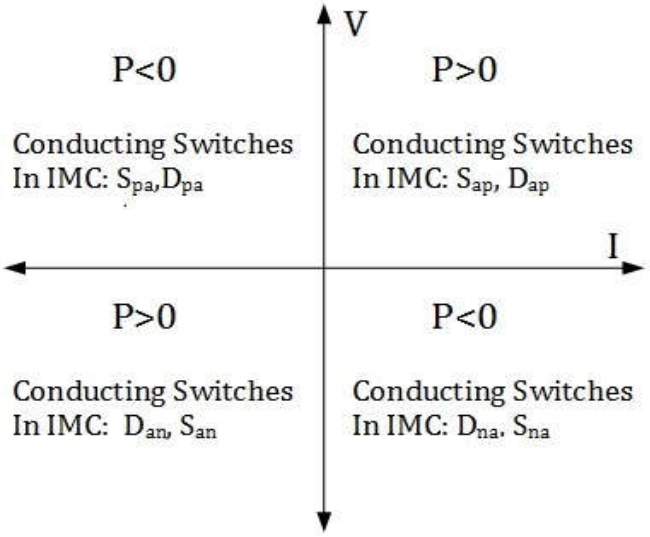

Fig. 2.2. Four quadrant power flow in IMC

MODULATION SCHEME

The modulation strategy is devised in such a way that the DC-Link Voltage is always positive. With reference to the symmetry of the circuit topology and an assumed symmetry of the three phases input voltage system the input voltage to the system can be considered as:

$$u_a = U_1 \cos(\theta)$$

$$u_a = U_1 \cos(\theta - 2\pi/3) \quad (3.1)$$

$$u_a = U_1 \cos(\theta + 2\pi/3)$$

$$u_a + u_b + u_c = 0$$

Where u_1 is the input peak amplitude and $\omega_1$is the angular frequency. In order to achieve maximum output voltage, a input phase is clamped to the positive or negative DC link bus for π/3 wide intervals when the corresponding phase voltage has highest value. The local average DC-Link voltage u is formed by taking the average of the upper and the lower envelope of the DC Link voltage u over a sample period T_P. At any instant the upper envelope of u is formed by the summation of absolute values of maximum and minimum of input phase values. For the period 0 - π/6 the DC-Link voltage is formed by the line voltage u_{ac} and u_{ab}. Similarly, for the period π/6 - π/3 the DC-Link voltage is formed by the line voltage u_{ac} and u_{bc}. The switching strategy has been designed in such a way that the switching of rectifier occurs at the time of inverter freewheeling state. In this way the Zero DC-Link Current Commutation is achieved. The switching pulses for a pulse period $t_\mu = 0....\pi/6$ for the rectifier and the inverter stage. In fig. 3.1 the time period T_P has been divided in two equal pulse periods of $T_p/2$. One $T_P/2$ pulse period has been again divided into $T_p/3$and $T_p/6$. To reduce the switching losses the sequence of applied vectors in a half pulse period i.e $t_\mu = 0.....T_p/2$, is repeated in a reverse direction for the another half pulse period i.e. $t_\mu = T_p/2...T_p$ as shown in Fig. 3.1.

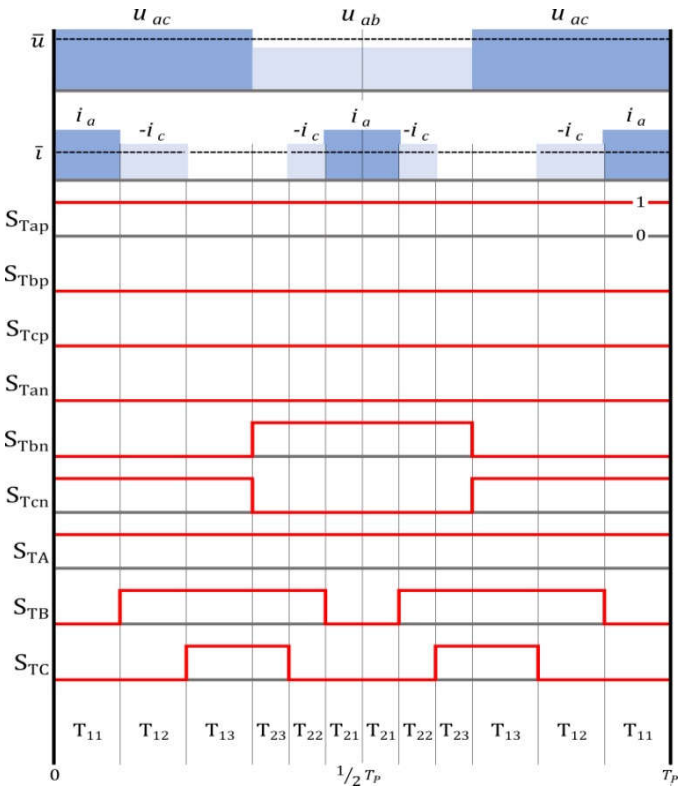

Fig. 3.1. Formation of voltage and current for DC-link

SWITCHING ALGORITHM

For the input to the Rectifier, $D_{ac} + D_{ab} = 1$ where, Dac and Dab are the relative on-time of the switches for generation of DC-Link voltage u = u_{ac} and u = u_{ab}. For the interval 0...π/6, input phase "a" is clamped to the positive DC-Link bus. The average current of the phases "a", "b", "c" are

$$i_a = (D_{ab} + D_{ac})i \;,\; i_b = -(D_{ab})i \;,\; i_b = -(D_{ac})i \quad (4.1)$$

The inverter output voltage, u_2 with an absolute value, and a phase value of $\varphi_2 = \omega_2 t = 0 - \pi/6$ is formed over a half pulse period $1/2T_P$ is

$$T_{ac} = \frac{D_{ac} T_p}{2}, \; T_{ab} = \frac{D_{ab} T_p}{2} \qquad (4.2)$$

For generating the reference vector, the location of the reference vector has to be identified. The Space Vectors of MC divide the space vector plane in six sectors and form a hexagon in inverter side as well as rectifier side. The coordination between inverter side hexagon and rectifier side hexagon is done in such way that the zero current switching in the rectifier side can be achieved. To get maximum and symmetrical DC-Link voltage, the each sector of 60^0 duration is divided into two sub-sectors of 30^0 duration. Depending on the reference vector angle on the Space vector hexagon the sub-sector selection has been done. After the identification of the sub-sector the reference vector is generated by applying the nearby vectors such that the harmonic distortions are less. The nearby vector is applied in such a way that the volt second balance can be achieved. Each nearby vector is applied for certain duration of pulse period. This time periods are known as dwell time period.

The reference vector is generated by applying the nearby vector in a sequence such that at the time of transition from one state to another only one switch on the inverter side as well as rectifier side gets switched. This whole vector sequence is occupied one pulse period. There needs to be introduced a variable which varies from $0...T_P$. On the other hand, the dwell times are divided between vectors according to vector sequence and in a symmetric manner. So, when the variable which is denoted by time 'T' is in between $0...T_{11}$ the vector-1 is applied. Similarly when the variable time the vector-2 is in between T_{11} to $T_{11} + T_{12}$ is supplied. The vector sequence for generating the reference vector is in such a way that the following condition should be maintained i.e. at the instant of transition from one vector to another vector only one switch gets switched. The switching of more than one switch is not permissible. To reduce the switching losses, the vector sequence for the first half of pulse period is repeated in reverse direction for the second half. The starting vectors should be the ending vector. According to the vector sequence the switching pulse will generate on the other hand according to the value of variable time "T" the vector sequence will be applied in a pulse period. According to the vector sequence the switching pulses for the Matrix Converter is generated. Out of these 18 switches the pulses for middle three switches of the rectifier side depends on the switching pulses for the other upper and the lower switches of the rectifier stage. So, each vector like V-1 generates 18 switching pulses is nothing but the elements of the column array x. when the any element of the column array is 1 that means that particular switching pulse is "HIGH". On the other hand if the element is x that particular switching pulse is "LOW". The main application of IMC here is to control the rotor current of DFIG with variable speed system. In this paper the DFIG fed by indirect space vector modulated matrix converter is taken. Only results of simulation are presented. The stator windings of DFIG are directly connected to grid and the rotor windings are connected to grid through the proposed converter called as indirect matrix converter. The IMC consist of GSC (works as current source inverter) and RSC (works as voltage source inverter).

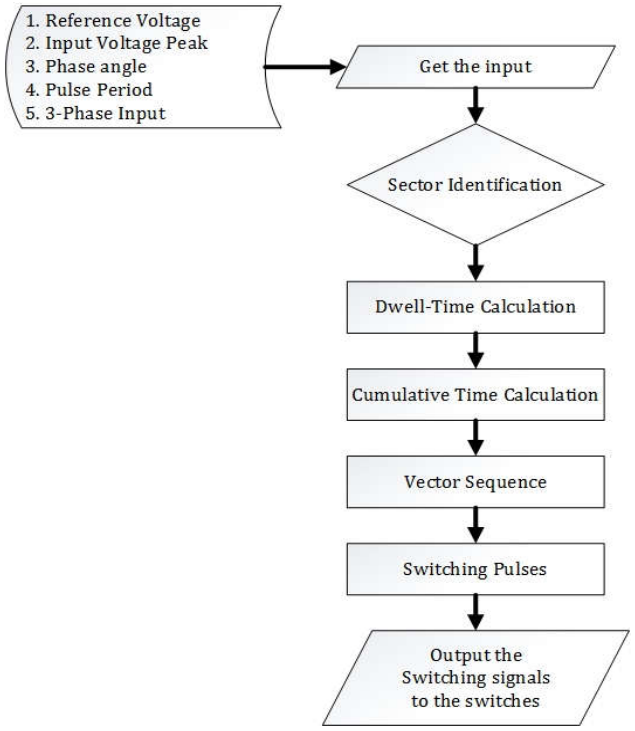

Fig. 4.1. Flow chart of modulation

IMC WITH AN APPLICATION IN WECS

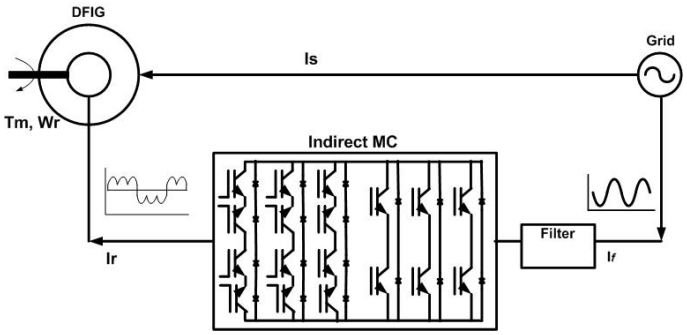

Fig. 5.1. Circuit diagram of DFIG with IMC

The system concept is that machine side converter (RSC) controls the speed by controlling the output current, which can be manipulated by the virtual dc-link by adjusting the input to GSC. Thus the power factor can be improved easily. Due to the bidirectional power flow of the converter the rotor circuit of DFIG able to work as a generator both in sub-synchronous and super-synchronous mode. Depending upon the mode of operation the power is either feed to or feed from the rotor. Rotor side converter used to generate or absorb power from grid in order to keep the voltage constant. In steady state we can assume the power of stator side is equal to the rotor power and in both sub-synchronous and super-synchronous mode rotor absorbs power from the converter. The modes are determined from the three phase voltage sequence of the generated rotor voltage. The frequency of this voltage is equal to the product of grid frequency and the absolute value of slip. If the slip value is negative the machine is running above synchronous speed in the direction of rotating field. If the slip is positive the machine has to be driven by a mechanical power to counteract the torque. It is called the generating mode of

machine. The both side converter have capability of generating or consuming reactive power from grid terminal.

RESULTS AND DISCUSSION

The output voltage is generated from the average DC-Link voltage which is given in equation. For the given specification, the average DC-Link voltage over the pulse period T_P (u) can be calculated as $u = \frac{3U_1}{2}\frac{1}{\cos \omega t}$ where ωt varies from 0 and π/6. And U_1 is the peak value of input. Therefore maximum and minimum value of average is 207.84v and 180v. $\overline{U}$ $\overline{U}$ is called as global average value of DC-Link. Therefore is 193.92v. Peak value of the output phase voltage is calculated as $\frac{2}{3}MU_1$ where M is modulation index, also the rms values can be found.

Table 6.1. Experimental specifications

1	Maximum input voltage (U_1)	120V
2	Fundamental Frequency (f)	50Hz
3	Rectifier Switching frequency (fswr)	10kHz
4	Inverter Switching Frequency (fswi)	20kHz
5	3-phase load	R-L load
6	Modulation technique	SVM

The simulation of the SMC has been done with 3-phase star connected R = 30Ω and L = 50mH with a modulation index of 0.8. The DC-link voltage varies between the maximum and the minimum values since it is formed by the voltage differences between two phases as discussed.

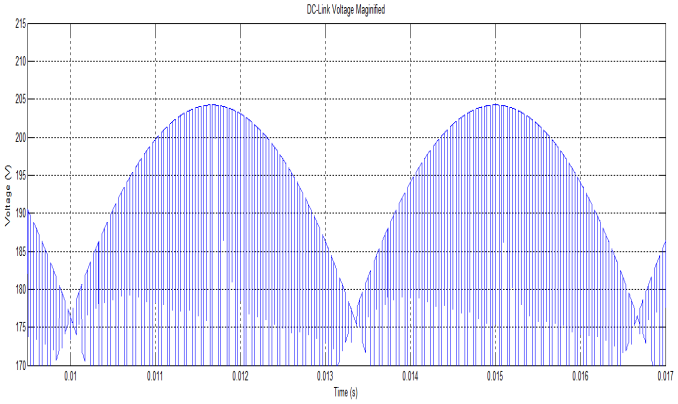

Fig. 6.1. DC-Link Voltage of SMC

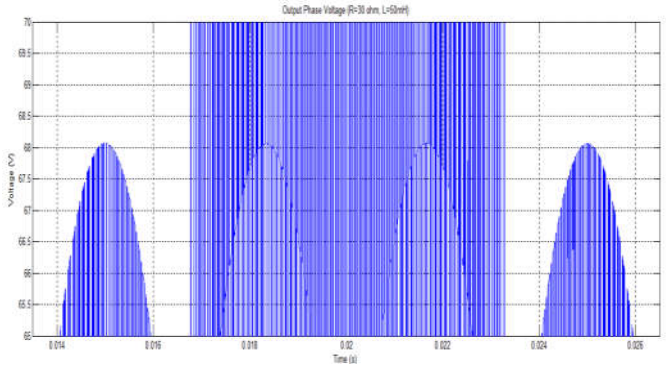

Fig. 6.2. Magnified positive side second level Peak Value of Output Phase Voltage

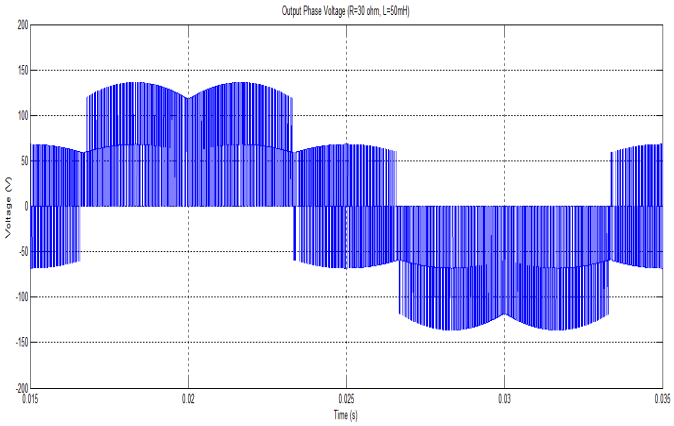

Fig. 6.3. One cycle of Output Phase Voltage of IMC

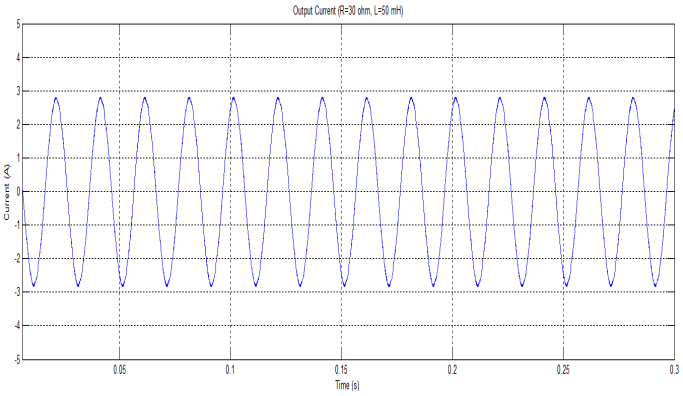

Fig. 6.4. Output Phase Current of IMC

Voltage stress across a switch is very important aspect that has to take care while designing any power electronic circuit. Depending on the voltage stress the lifespan and the rating of the switching device needs to be decided.

The voltage stress cross the rectifier switches connected to the positive DC-Link bus (Spi) is shown in as shown in figure. The same nature with negative voltage will be obtained in the case of switches connected to the negative DC-Link bus.

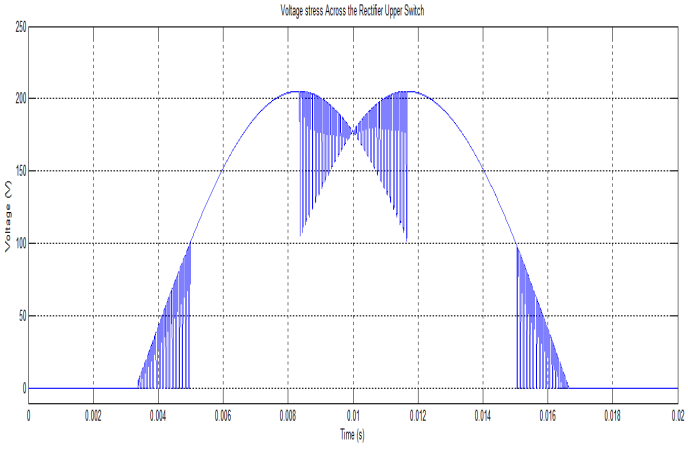

Fig. 6.5. Voltage Across Rectifier Upper Switch in IMC

The peak of the voltage stress across the switches S_{pi} is u_{max} = 207.84v. The nature of voltage stress across the rectifier middle switch of each phase is shown in fig. 6.5.

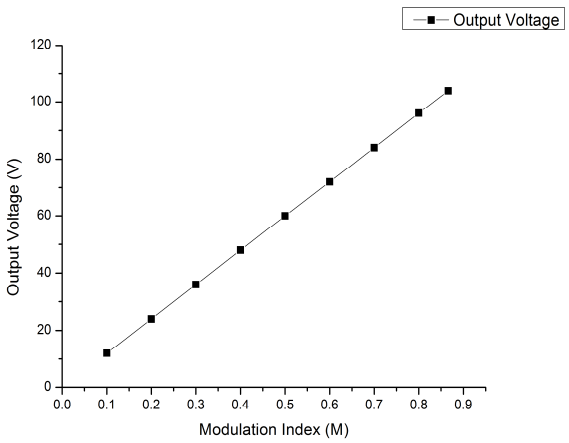

Fig. 6.6. Behaviour of output voltage with various modulation index

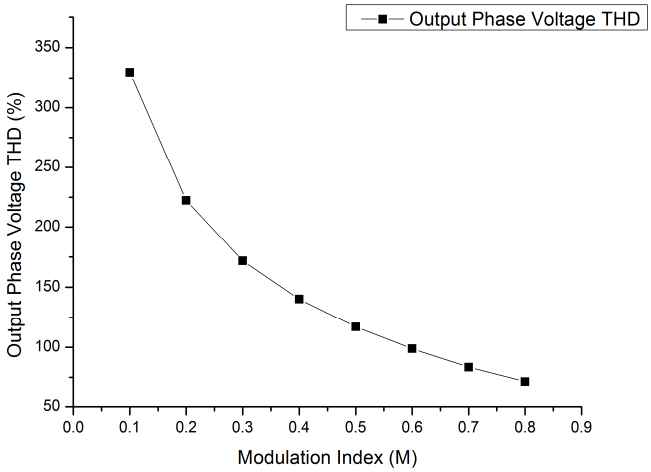

Fig. 6.6. Behaviour of THD with various modulation index

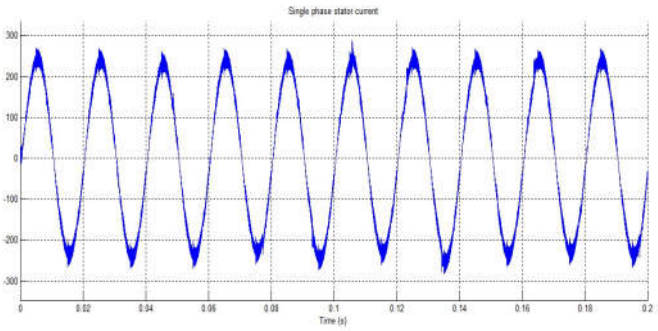

Fig. 6.7. Single phase stator current of DFIG

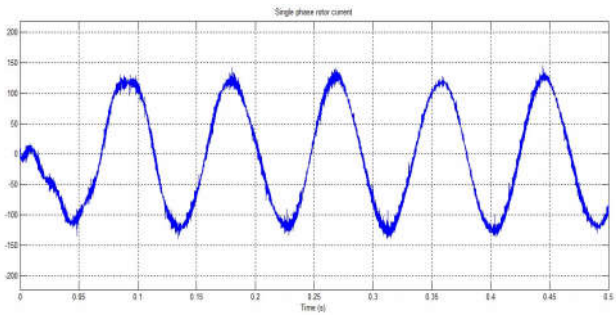

Fig. 6.8. Single phase rotor current of DFIG

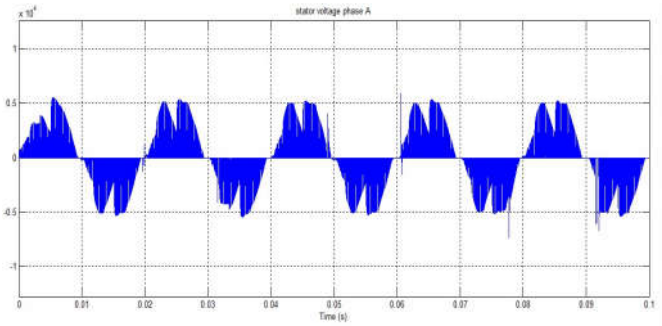

Fig. 6.9. Single phase stator voltage of DFIG

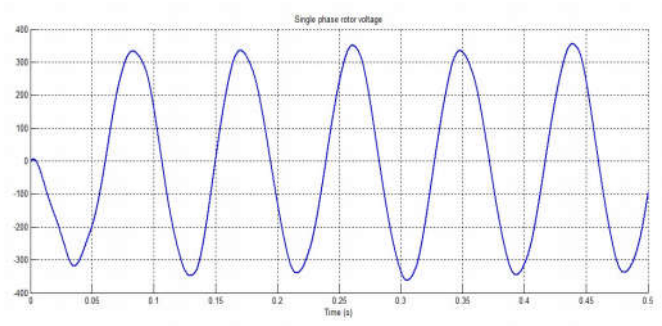

Fig. 6.10. Single phase rotor voltage of DFIG

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